Handout

Subject Name: Digital System Design

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Year and Sem, Department:II Year I Sem,ECE

Unit-I: (**Number System & Boolean Algebra**)

Important points / Definitions: (Minimum 15 to 20 points covering complete topics in that unit)

➢ Number system is a basis for counting varies items. Modern computers communicate and operate with binary numbers which use only the digits 0 &1. Basic number system used by humans is Decimal

➢ The human beings use decimal number system while computer uses binary number system. Therefore it is necessary to convert decimal number system into its equivalent binary

➢ In digital computers to simplify the subtraction operation & for logical manipulation complements are used. There are two types of complements used in each radix system (r,r-1)

➢ Binary codes are codes which are represented in binary system with modification from the original ones

➢ A code is said to be reflective when code for 9 is complement for the code for 0, and so is for 8 and 1 codes, 7 and 2, 6 and 3, 5 and 4. Codes 2421, 5211, and excess-3 are reflective, whereas the 8421 code is not

➢ A code is said to be sequential when two subsequent codes, seen as numbers in binary representation, differ by one. This greatly aids mathematical manipulation of data. The 8421 and Excess-3 codes are sequential, whereas the 2421 and 5211 codes are not.

➢ The gray code is a reflective digital code which has the special property that any two subsequent numbers codes differ by only one bit

➢ The simplest techniques for detecting errors is that of adding an extra bit known as parity bit to each word being transmitted.Two types of parity**:** Oddparity**,** even parity

➢ A code is said to be an error -correcting code, if the code word can always be deduced from an erroneous word

➢ Alphanumeric codes are ASCII code & EBCDIC code.

➢ Boolean algebra is a system of mathematical logic. It is an algebraic system consisting of the set of elements (0, 1), two binary operators called OR, AND, and one unary operator NOT. It is the basic mathematical tool in the analysis and synthesis of switching circuits

➢ **Commutative law** Law1: A+B=B+A Law2: A.B=B.A

➢ **Associative law** Law1: A + (B +C) = (A +B) +C Law2: A(B.C) = (A.B)C

➢ **Distributive law** Law1: A.(B + C) = AB+ AC Law2: A + BC = (A + B).(A +C)

➢ **Consensus Theorem** Theorem1. AB+ A'C + BC = AB + A'C Theorem2. (A+B).(A'+C).(B+C) =(A+B).(A'+C)

Short Questions (Minimum 10 previous JNTUH Questions – Year to be mentioned)

1. What is diminished radix complement(May 2019)
2. What is Gray code? (Dec 2018)
3. Distinguish between canonical and standard forms by giving an example(Dec 2017)
4. How do you obtain dual of an expression(Dec 2018)
5. Construct AND, OR and NOT gate using universal gates (May 2018)
6. What are the basic operations of Boolean Algebra(Dec 2014)
7. Implement Ex-OR with NAND gates(May 2018)
8. What are the simplest technique used for detecting errors(Dec 2016)
9. Find the 2s complement of -7 **(May 2015)**
10. Implement Ex-NOR gate using only NAND gates (Dec 2016)

Long Questions (Minimum 10 previous JNTUH Questions – Year to be mentioned)
1. Covert 105.15_{10} to binary, octal, hexadecimal (Dec 2018)
2. With an example show how Hamming Code can be used to correct single error (April 2018)
3. What are the various logic gates, give the representation along with the truth table.
   b) What is the use of complements? Perform subtraction using 7's complement for the given Base-7 numbers (565)-(666). (Dec 2017)
4. Generate 4 bit gray code directly using mirror image property (Dec 2018)
5. Convert $(657)_8$ into decimal.
   Convert $(2348)_{10}$ into hexa decimal(May 2018)
6. Convert 110001.1010010 into hexadecimal. Convert $(423.25)_{10}$ into Hex.
   Simplify A(B+C)+AB+ABC
   Write the truth table and symbols of AND and OR gates(May 2018)
7. Convert the hexadecimal number 64CD H to binary and then convert it from binary to octal (Jun 2019)
8. Write the properties of XOR gates.
   Convert $(A0F9.0EB)_{16}$ to decimal, binary, octal (May 2019)
9. Using 2's complement perform $(42)_{10} – (68)_{10}$. (Dec 2016)
10. Implement the function with AND, OR, and NOT gates given the Boolean expression
    F= x y + x' y' + y' z.
    Discuss the basic theorems of Boolean algebra with necessary proofs (Dec 2018)

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)
1. The A+A'B= **A+B**
2. Excess -3 Code of 9 is **1100**
3. Universal Gates are **Nand & Nor**
4. Nibble : **4 Bits**
5. Abbreviate ASCII **American Standard Code for Information Interchange**
6. Self Complementing Code :**2421,Excess-3**
7. BCD Means :**Binary Coded Decimal**
8. Consensus Theorem : **AB+ A'C + BC = AB + A'C**
9. Encode ECE in ASCII : **(100 0101 100 0011 100 0101)**
10. Duality Theorem : **A.A' =0 ,A+A'=1**

Unit-II: (**Minimization of Boolean functions & Combinational Logic Circuits**)
Important points / Definitions: (**Minimum 15 to 20 points covering complete topics in that unit**)

- ❖ The process of simplifying the algebraic expression of a boolean function is called **minimization**
- ❖ Group May be Horizontal,Vertical But not Diagonal
- ❖ After grouping the cells ,the sum terms which appear in the K-Map are called as Prime Implicant groups
- ❖ Don't Care Conditions may be taken into Consideration or not for minimization technique
- ❖ SOP(Sum of Products),POS (Product of Sums) are the Canonical Forms
- ❖ Combination Circuit does not have Feedback and depend on Input Values
- ❖ Full Adder is the Circuit which adds the 3 Bits & gives output as Sum ,Carry
- ❖ Parallel adder is Ripple carry adder in which carry output of each full adder in connected to the carry input of next higher order Stage
- ❖ Magnitude comparator is the Circuit which Compares the magnitude of two binary numbers
- ❖ Decoder used in Code Converters,BCD to Segment Display,Address Decoding
- ❖ Each square or rectangle made up of the bunch of adjacent minterms is called a subcube.
- ❖ Each of these subcubes is called a Prime implicant
- ❖ The PI which contains at leastone which cannot be covered by any other prime implicants is called as Essential Prime implicant (EPI).

Short Questions (**Minimum 10 previous JNTUH Questions – Year to be mentioned**)

1. How many adjacent cells are there to each cell in a n variable K-map(May 2019)
2. What is Minterms and Maxterms(May 2019)
3. Write the truth table of half adder (May 2018)
4. Draw half subtractor circuit (May 2018)
5. Compare a decoder with a demultiplexer(Dec 2018)
6. Define combinational circuits and give examples.(May 2018)
7. Differentiate between combinational and sequential circuits(May 2018)
8. Draw the diagram of 4-Bit Parallel adder cum parallel subtractor.(Dec 2017)
9. What is code converter? (Dec 2016)
10. Explain about Multiplexers with three-state gates (June 2019)

Long Questions (**Minimum 10 previous JNTUH Questions – Year to be mentioned**)

1. Minimize the following expressions using K-map and realize using NAND Gates.
   $f = \Sigma m (1,3,5,8,9,11,15) + d (2,13)$ (May 2019)
2. Express the complement of the following function F in sum of minterms form
   $F(A,B ,C, D) = \Sigma(2, 4, 7, 10, 12, 14)$
   Show that the dual of the exclusive OR is equal to its complement(June 2019)
3. Design half adder using only NAND gates.
   Design a combinational circuit which converts BCD to Excess-3 code.(May 2018)
4. Find all the prime implicants for the Boolean function.
   $F(w,x,y,z)=\Sigma(0,2,4,5,6,7,8,10,13,15)$ and find which are essential.
   Simplify $BD+BCD'+AB'C'D'$ and implement using two level NAND gates(April 2018)
5. Derive the product of maxterms for $f(a,b,c,d)=a.b.c+ b'.d+c.d'$.
   Derive and Implement Exclusive OR function involving three variables using only NAND function(May 2017)
6. Draw a NAND logic diagram that implements the complement of the following function:
   $F(A,B,C,D) = \Sigma(0, 1, 2, 3, 6, 10, 11, 14)$.
   Find the minterms of the following Boolean expressions by first plotting each function in a map: (i) xy + yz + xy'z (ii) C'D + ABC' + ABD' + A'B'D(May 2019)

7. Design and implement a Full adder using two half adders and OR gate(Dec 2018)
8. Design a 4:16 decoder using 3:8 decoders with its structural diagram(Dec 2018)
9. What is Multiplexer? Implement a full subtractor with two 4×1 multiplexers (Dec 2018)
10. Design a combinational circuit with three inputs, x, y and z and three outputs, A, B and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input (May 2019)
11. Design a 2 bit magnitude comparator.
    Implement 4*16 decoder using two 3*8 decoders(April 2018)
12. Construct 4×16 line decoder using 3×8 line decoders.
    Design a BCD to Excess-3 code convertor(April 2018)

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)
1. Full Adder Consists of Xor Gate and And Gate
2. Multiplexer has n Selection lines
3. The gate used at the ouput of SOP Function is Or Gate
4. The number of Combinations used in n variable function is 2^n
5. **Quad** is a group of four adjacent cells in K Map
6. Diagonal Grouping in K-Map is called as **Illegal gouping**
7. **Priority Encoder** is an encoder circuit that includes the priority function
8. Number of data ouputs in demultiplexer **is** 2^n
9. Application of Multiplexer is i) Data selector ,Frequency Multiplexing
10. Alternate Name of Tabular Method is **Quin Mc –Cluskey Method**

Unit-III: (Sequential Circuits Fundamentals & Registers and Counters)
Important points / Definitions: (Minimum 15 to 20 points covering complete topics in that unit)

- Sequential circuits are divided into two main types: **synchronous** and **asynchronous**
- *Synchronous* sequential circuits change their states and output values at discrete instants of time, which are specified by the rising and falling edge of a free-running **clock signal**
- Latches and flip-flops are the basic elements for storing information. One latch or flipflop can store one bit of information
- There are basically four main types of latches and flip-flops: SR, D, JK, and T.
- The characteristic equation of the JK flip-flop is $Q^* = J.Q' + K'.Q$
- **Propagation Delay Time:** is the interval of time required after an input signal has been applied for the resulting output change to occur
- **Set-up Time: i**s the minimum interval required for the logic levels to be maintained constantly on the inputs (J and K, or S and R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop
- **Applications of flip-flops is** Frequency Division**,** Parallel data storage, Serial data storage
- The Master-Slave Flip-Flop is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from Q and Q from the "Slave" flip-flop are fed back to the inputs of the "Master" with the outputs of the Master" flip-flop being connected to the two inputs of the "Slave" flip-flop
- **shift register** is a cascade of flip-flops sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it

- Shift registers can have both parallel and serial inputs and outputs. These are often configured as **serial-in, parallel-out** (SIPO) or as **parallel-in, serial-out** (PISO)
- A bidirectional shift register is one which the data bits can be shifted from left to right or from right to left
- If the register has both shifts and parallel load capabilities, it is referred to as a universal shift registers
- **Counter** is a device which stores (and sometimes displays) the number of times particular event or process has occurred, often in relationship to a clock signal
- Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops
- Up/down counter – counts both up and down, under command of a control input
- Ring counter – formed by a shift register with feedback connection in a ring
- Johnson counter – a *twisted* ring counter

Short Questions (Minimum 10 previous JNTUH Questions – Year to be mentioned)
1. Compare latch and flip flop (June 2019)
2. List out the drawbacks of ripple counters (June 2019)
3. Define the following terms of a flip flop
   Hold time ii) Set up time iii) Propagation delay time
4. Draw the circuit diagram of Ring counter (April 2018)
5. Explain clear and preset inputs (April 2016)
6. Compare synchronous and Asynchronous counters (Nov 2016)
7. What is race around condition (Nov 2016)
8. What are the basic types of shift register (Nov 2018)
9. Show the excitation table and truth table of JK flip flop(Nov 2017)
10. Explain about characterstic equation for jk flip flop (June 2019)

Long Questions (Minimum 10 previous JNTUH Questions – Year to be mentioned)
1. Explain the operation of R-S master slave flip flop. Explain its truth table(June 2019)
2. Explain the operation of clocked SR flip-flop with its characteristic table. (Dec 2018)
3. Design and explain Johnson counter ,Explain 3-bit Ripple Counter (April 2018)
4. Realize D-FF and T-FF using JK-FF. Draw the logic diagrams with their truth tables (Dec 2016)
5. Draw and explain the circuit diagram of positive edge triggered J-K flip-flop using NOR gates with its truth table. How race around conditions are eliminated? (Dec 2018)
6. What do you mean by universal shift register? Draw and explain its circuit diagram and operation (Dec 2018)
7. Design a 4-bit Ring Counter. b) Design a T flip-flop using JK flip-flop. Use k-maps for the design(May 2018)
8. Explain the operation of 4-bit Johnson counter using D-flip flops with the help of bit pattern(Nov 2018)
9. Design a 4 bit synchronous counter with D flip - flops and explain its working(May 2019)
10. Discuss the design procedure for the clocked sequential circuits(Dec 2018)

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1. **Maximum Clock Frequency** is the highest rate that a flip-flop can be reliably triggered
2. **Level Trigger** is used in Latch
3. Register is the device which stores group of information
4. serial in-serial out (SISO) **shift registers**, in which data is input serially until it reaches the output
5. Serial adder is the adder used in Sequential Circuit
6. Applications of Flipflop : Frequency Division**,** Parallel data storage, Serial data storage
7. *Synchronous* sequential circuits change their states and output values at discrete instants of time, which are specified by the rising and falling edge of a free-running clock signal
8. Alternative name of Asynchronous Counter is Ripple Counter
9. D Flip Flop is used in Buffer Register
10. Universal Shift Register is the register which has both right ,Left Shft and also Parallel Load Capabilities

Unit-IV : (Sequential Machines)

Important points / Definitions: (Minimum 15 to 20 points covering complete topics in that unit)

- Sequential circuits are also called finite state machines (FSMs).
- The state diagram or state graph is a pictorial representation of the relationships between the present state, the input, the next state, and the output of a sequential circuit
- In case of moore circuit ,the directed lines are labeled with only one binary number representing the input that causes the state transition
- A sequence detector is a sequential machine which produces an output 1 every time the desired sequence is detected and an output 0 at all other times
- Finite state machine can be defined as a type of machine whose past histories can affect its future behavior in a finite number of ways
- Mealy type model: in this model, the output is a function of the present state and the present input
- Redundant states are states whose functions can be accomplished by other States
- Two states are said to be equivalent. When two states are equivalent, one of them can be removed without altering the input output relationship
- State equivalence theorem: it states that two states s_1, and s_2 are equivalent if for every possible input sequence applied
- The merger graph is a state reducing tool used to reduce states in the incompletely specified machine
- Synchronous counters are counters in which all the flip flops are triggered simultaneously by the clock pulses
- The state diagram showing all the possible states state diagram which also be called nth transition diagrams, is a graphical means of depicting the sequence of states through which the counter progresses
- The required number n of the flip-flops- the smallest value of n is such that the number of states $N \leq 2^n$

Short Questions (Minimum 10 previous JNTUH Questions – Year to be mentioned)
1. What are capabilities of finite state machine(June 2019)
2. Define: i) State table ii) State Diagram (Nov 2018)
3. Compare Mealy and Moore machines (Nov 2018)
4. What do you mean by State table?(March 2017)
5. How do you obtain the maximal compatibles from the merger table(March 2017)
6. State the rules of state assignment**?**
7. Define State reduction**?**
8. When does sequential machine said to be strongly connected**?**
9. Define Serial binary adder**?**
10. What is Modulo-N Counter?

Long Questions (Minimum 10 previous JNTUH Questions – Year to be mentioned)
1. Design, draw and explain a synchronous MOD-12 down-counter using J-K flip-flop (June 2019)
2. Explain the differences between asynchronous and synchronous counters. Design a MOD-10 ripple counter (June 2019)
3. Compare Mealy and Moore machines.
   Explain the procedure for state minimization using merger graph and merger table with example (June 2019)
4. Design and construct MOD-5 synchronous counter using JK flip flops (June 2019)
5. Design divided by 6 ripple down counter that counts down from 7 and use flip flops that are toggle on positive to negative transitions, and take outputs off the Q lead(March 2017)
6. Define state, state diagram. Draw state diagram taking any one as an example (Nov 2016)
7. Design a 3-bit up/down counter which counts up when the control signal M=1 and counts down when M=0. (Nov 2016)
8. Design a 4 bit synchronous counter using JK flip flops. (March 2017)
9. Design decade Counter using JK Flip Flop?
10. Design Sequence detector which can detect 101?

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)
1. A state diagram is a type of diagram used in computer science and related fields to describe the behavior of systems
2. A mealy machine is defined as a machine in theory of computation whose output values are determined by both its current state and current inputs
3. Modulo N Counter   is a counter which counts the repeated sequence of N
4. The serial binary adder or bit-serial adder is a digital circuit that performs binary addition bit by bit
5. A moore machine is defined as a machine in theory of computation whose output values are determined only by its current state
6. Finite state machine can be defined as a type of machine whose past histories can affect its future behavior in a finite number of ways
7. Sequential circuits are also called finite state machines
8. A sequence detector is a sequential machine which produces an output 1 every time the desired sequence is detected and an output 0 at all other times
9. A state table is one of many ways to specify a state machine, other ways being a state diagram, and a characteristic equation
10. A moore machine is defined as a machine in theory of computation whose output values are determined only by its current state

Unit-V : (Realization of Logic Gates Using Diodes & Transistors) (New)

Important points / Definitions: (**Minimum 15 to 20 points covering complete topics in that unit**)

- Discrete OR gates may be realized by using diodes or transistors
- In the positive logic system, higher of the two voltage levels are represented as 1 and lower of the two voltage levels are represented as 0
- In the negative logic system, higher of the two voltage levels are represented as 0 and lower of the two voltage levels are represented as 1
- Transistor-transistor logic (TTL) is a digital logic design in which bipolar transistors act on direct-current pulses
- Noise margin is a measure of design margins to ensure circuits functioning properly within specified conditions. ... The noise margin, $NM_H = |V_{OH\ min} - V_{IH\ min}|$, for logical high
- Fan-in is a term that defines the maximum number of digital inputs that a single logic gate can accept
- The maximum fan-out of an output measures its load driving capability.
- Resistor-Transistor Logic, or RTL, refers to the obsolete technology for designing and fabricating digital circuits that employ logic gates consisting of nothing but transistors and resistors
- The voltage difference between the logic levels used for 1 and 0 is termed as Logic Swing
- A transmission gate (TG) is an analog gate similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential
- TTL integrated circuits (ICs) were widely used in applications such as computers, industrial controls, test equipment and instrumentation, consumer electronics, and synthesizers
- The TTL "totem-pole" output structure often has a momentary overlap when both the upper and lower transistors are conducting, resulting in a substantial pulse of current drawn from the power supply.

Short Questions (**Minimum 10 previous JNTUH Questions – Year to be mentioned**)

1. Define logic Gate & Logic Family?
2. Draw the circuit of Totem-pole TTL NAND gate (Dec 2018)
3. Define Noise Margin and fan out (June 2019)
4. What are the defining characteristics of digital logic families (Dec 2018)
5. Which of the parameters decide the fan out and how (Dec 2017)
6. Define Positive Level and Negative Level?
7. What are the demerits of TTL?
8. Draw CMOS Inverter Circuit?
9. What are the advantages of MOS over bipolar Logic Familes?
10. State advantages of CMOS Logic Family?

Long Questions (**Minimum 10 previous JNTUH Questions – Year to be mentioned**)

1. Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin, and propagation delay and fan-out (Dec 2018)
2. Draw ECL Nor Gate?
3. Draw CMOS 2-Input Nand Gate?
4. Draw and explain the working of two input TTL NAND gate and list advantages of totem Pole output stage
5. Draw CMOS 2-Input Nor Gate?
6. Draw and explain Circuit of AND,OR Using Diode ?
7. Explain Interfacing of Cmos With TTL ,TTL With Cmos?
8. Draw RTL Based AND,OR Gate?
9. Compare the difference between all Logic Families with all Parameters?

10. Draw and explain 2- Input AND,Or & Inverter Using CMOS ?

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1. Abbreviate CMOS Complementary Metal Oxide Semiconductor
2. Positive Logic Level   is the higher of the two voltage levels are represented as 1 and lower of the two voltage levels are represented as 0
3. The stages in TTL Nand Logic i) Diode And Gate & Input Protection ii) Phase Splitter iii)Output Stage
4. **Figure of merit**" (FOM) is a way of evaluating FETs. It accounts for both their conduction losses and their switching losses
5. **Fanout is number of gate inputs that are connected to single gate input**
6. **The Current flowing from source to Ouput under TTL Ouput is high Called as Source Current**
7. **ECL Stands as Emitter Coupled Logic**
8. **Buffer(4050B) is the device which is used to interface CMOS & TTL Under Low State Voltages**
9. **when transistors are used as basic building blocks of Logic Family ,then the Family is called as TTL**
10. Noise margin is a measure of design margins to ensure circuits functioning properly within specified conditions